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S H A R P C O R P O R A T I O N

SPEC I F I C A T I O N

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A P P L I C A B L E D I V I S I O N

[REDACTED] ; ; ; E; ANEL DEVELOPMENT

TFT DEVELOPMENT CENTER

LCD PRODUCTS DEVELOPMENT
C E N T R E

IEL PRODUCTION DEPT.

SPECIFICATION FOR
Passive Matrix LCD Module

Model No.

L M 3 2 K 0 7 1

CUSTOMER'S APPROVAL

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BY _____

PRESENTED

BY

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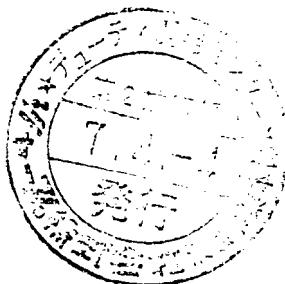
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SHARP Corporation



SHARP RECORDS OF REVISION			MODEL No.	LM32K071
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1. Application

This data sheet is to introduce the specification of **LM32K071**, Passive Matrix type LCD module.

2. Construction and Outline

Construction: 320X240 dots graphic display module consisting of a LCD panel, PWB(printed wiring board) with electric components mounted onto, TAB(tape automated bonding) to connect the LCD panel and PWB electrically, and plastic chassis with CCFT back light and bezel to fix them mechanically.

Outline See Fig. 7

Connection See Fig. 7 and Table 6.

3. Mechanical Specifications

Table 1

Parameter	Specifications	Unit
Outline dimensions Note 1)	170 (W) ×110 (H) ×8 MAX (D)	mm
Viewing area	121 (W) X91.6 (H)	mm
Active area	115 .17 (w) x86.37(H)	mm
Display format	320(W) X240(H)	
Dot size	0.33 (W) x0.33(H)	mm
Dot spacing	0.03	mm
Base color Note 2)	Normally white	Note 3)
Mass	Approx 220	g

Note 1) Excluded the mounting portions and connectors.

Note 2) Due to the characteristics of the LC material, the colors vary with environmental temperature.

Note 3) Positive-type display

Display data "H" : ON → Black

Display data "L" : OFF White

4. Absolute Maximum Ratings

4-1 Electrical absolute maximum ratings

Table 2

Parameter	Symbol	MIN.	MAX.	Unit	Remark
Supply voltage (Logic)	VDD-VSS	0	6	v	Ta=25 °C
Supply voltage (LCD)	VDD-VO	0	30	v	Ta=25 °C

4-2 Environmental Conditions

Table 3

Item	Tstg.		Topr.		Remark
	MIN.	MAX.	MIN.	MAX.	
Ambient temperature	-25 °C	+70 °C	-10 °C	+60 °C	Note 4) Note 5)
Humidity	Note 1)		Note 1)		No condensation
Vibration	Note 2)		Note 2)		3 directions (x/Y/z)
Shock	Note 3)		Note 3)		6 directions ($\pm X \pm Y \pm Z$)

Note 1) Ta≤40°C 95 % RH Max.

Ta>40 °C Absolute humidity shall be less than
Ta=40 °C/95 % RH.

Note 2)

Table 4

Frequency	10 Hz-57 Hz	57 Hz~500 Hz
Vibration level		9.8 m/s ²
Vibration width	0.075 mm	
I Interval	10 Hz-500 Hz-10 Hz/n min	

2 h for each direction of X/Y/Z (6 h as total)

Note 3) Acceleration : 490 m/s²

pulse width : 11 ms

3 times for each direction of $\pm X/\pm Y/\pm Z$

Note 4) Care should be taken so that the LCD module may not be subjected to the temperature out of this specification.

Note 5) There could be a case of the CCFT lamp not to discharge (light) at the low ambient temperature of below 0 °C.

5. Electrical Specifications

5-1 Electrical characteristics of LCD pane 1

Table 5

T_a=25 °C, VDD=5 V±5 %

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage (Logic)	VDD-VSS	Note 1)	4.75	5	5.25	v
Supply voltage (LCD drive)	VSS-VEE		-25.2	-24	-22.8	v
LCD contrast adjust voltage	VDD-V0	T _a =-10 °C	22.9	25.5	28.1	v
		T _a =+25 °C	19.8	22.1	24.4	v
		T _a =+60 °C	17.3	19.7	21.6	v
Input signal voltage	VI N	"H" level	0.8VDD	-	VDD	v
		"L" level	0		0.2VDD	v
Input leakage current	IIL	"H" level			20	μA
Supply current (Logic)	IDD	Note 2)		9	18	mA
Supply current (LCD)	IEE			7.2	14.4	mA
Power consumption (LCD)	Pd			218	327	mW

Note 1) The viewing angle θ at which the optimum contrast is obtained can be set by adjusting VDD-V0.

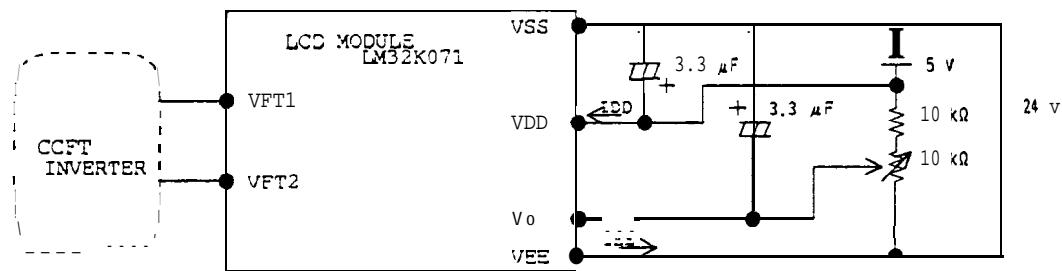
Note 2) Under the following condition.

VDD-VSS=5.0 v, VEE-VSS=-24.0 v, VDD-V0=22.1 v

Frame frequency=80 Hz

Display pattern=1bit checker

- Display pattern
- manamabumuanmnnumn9nmusu=n9amnma
 - umamamnmomamamnmomnmamumama9um
 - BnmamnmnmamaBamamamnm09n=n



CN2

CN1

5-2 Interface signalsTable 6-1 CN1

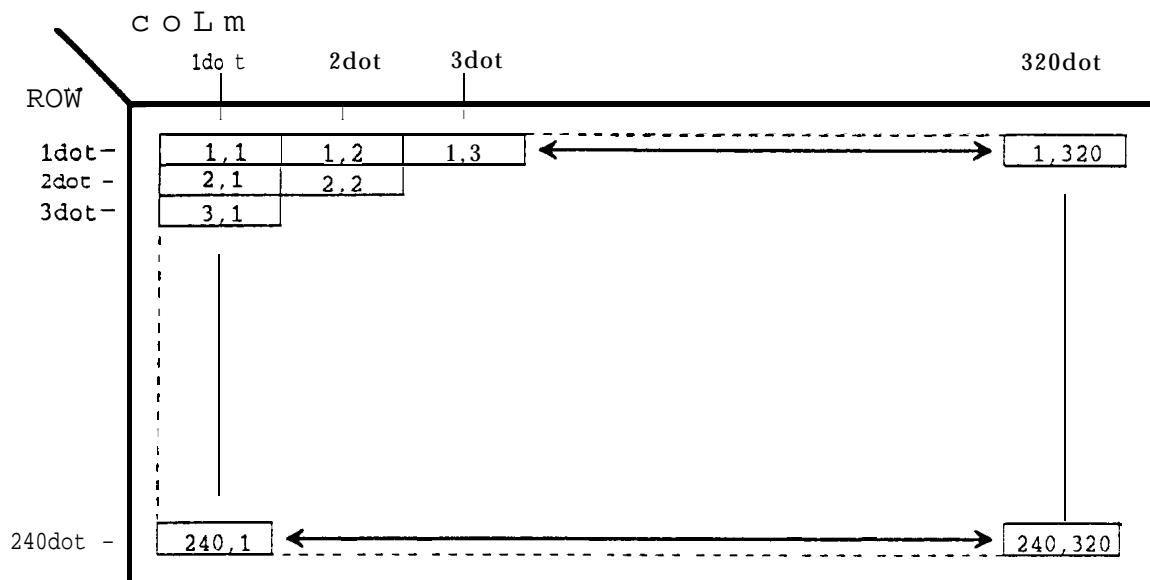
Pin No	Symbol	Description	Level
1	V0	LCD contrast adjust voltage	
2	VEE	Power supply for LCD	
3	D3		
4	D2	Display data signal	H(ON), L(OFF)
5	D1		
6	DO		
7	NC		
8	Vss	Signal ground	
9	VDD	Power supply for Logic	
10	CP2	Data input clock signal	"H"-->"L"
11	CP1	Input data latch signal	"H"-->"L"
12	s	Scan start-up signal	"H"

Used Cable : 1.25 mm pitch, 12 pins F.F. C

Table 6-2 CN2

Pin No	Symbol	Description
1	VFT 1	Power supply for CCFT back light
2	VFT 2	Power supply for CCFT back light

Pin No. and its location are shown in fig. 7.



COLUMN Note) 1,2 means 1st row 2rid column dot.

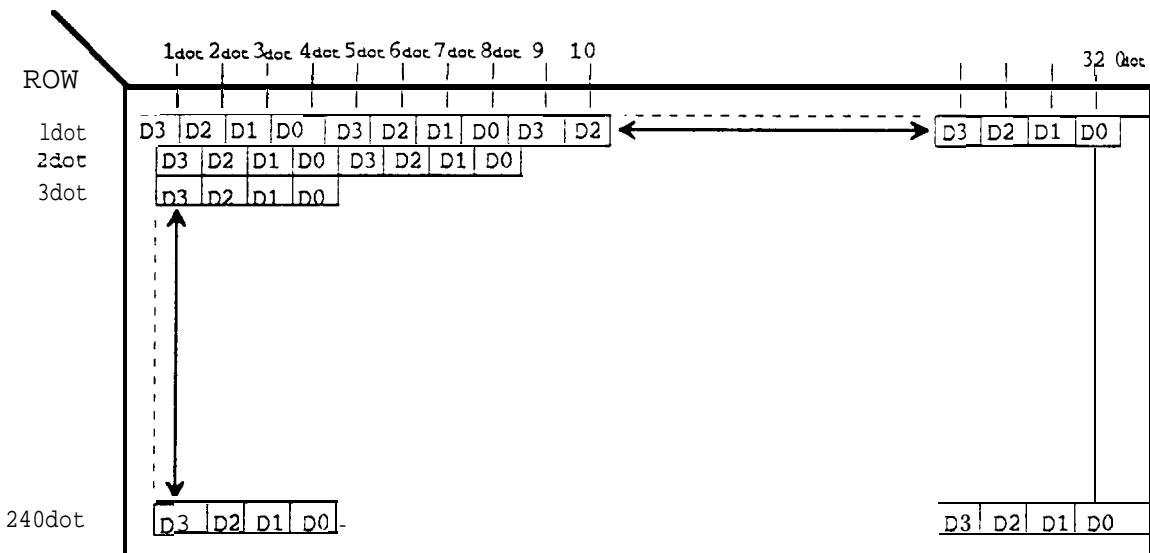


Fig.1 Dot chart of display area

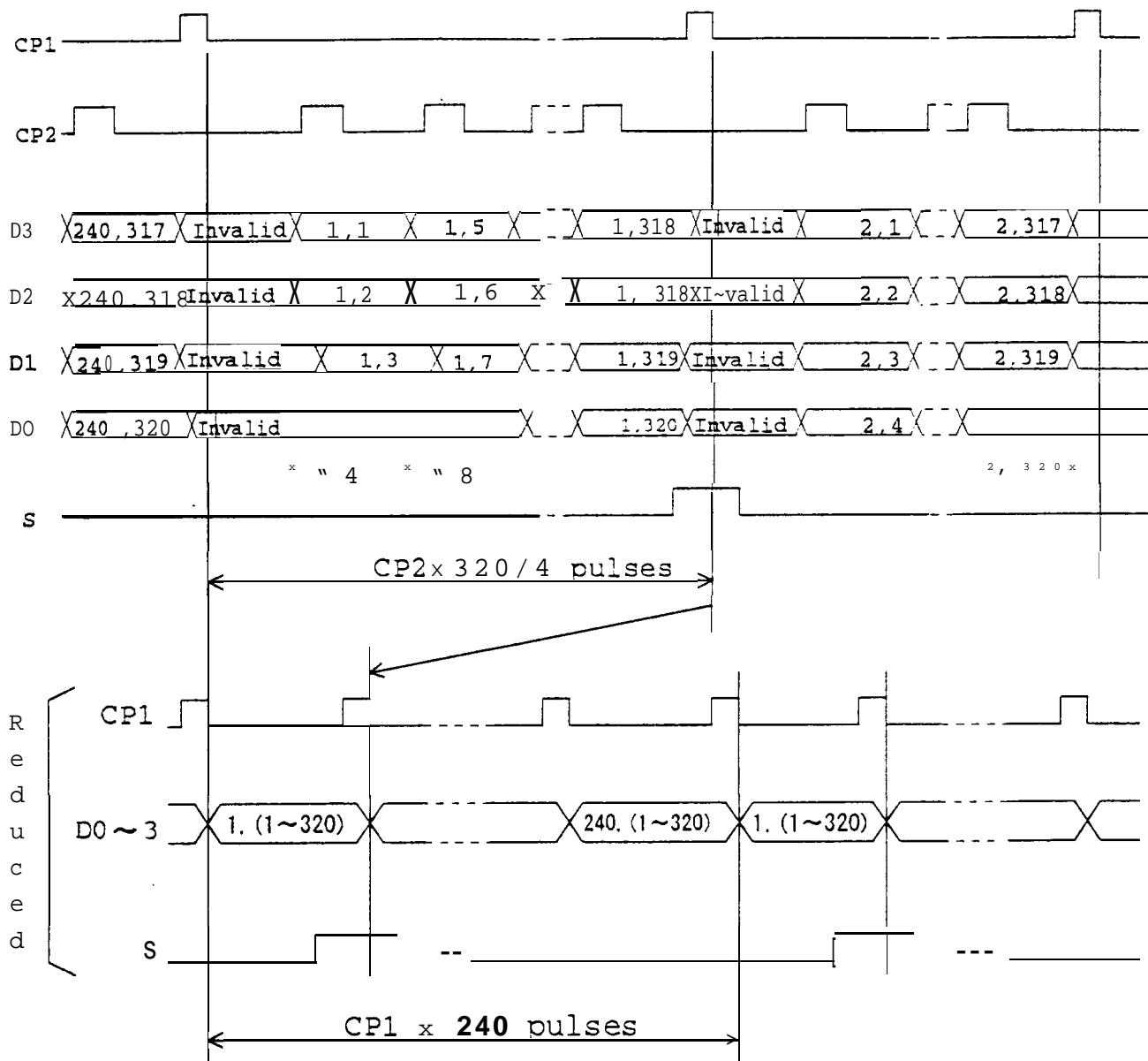
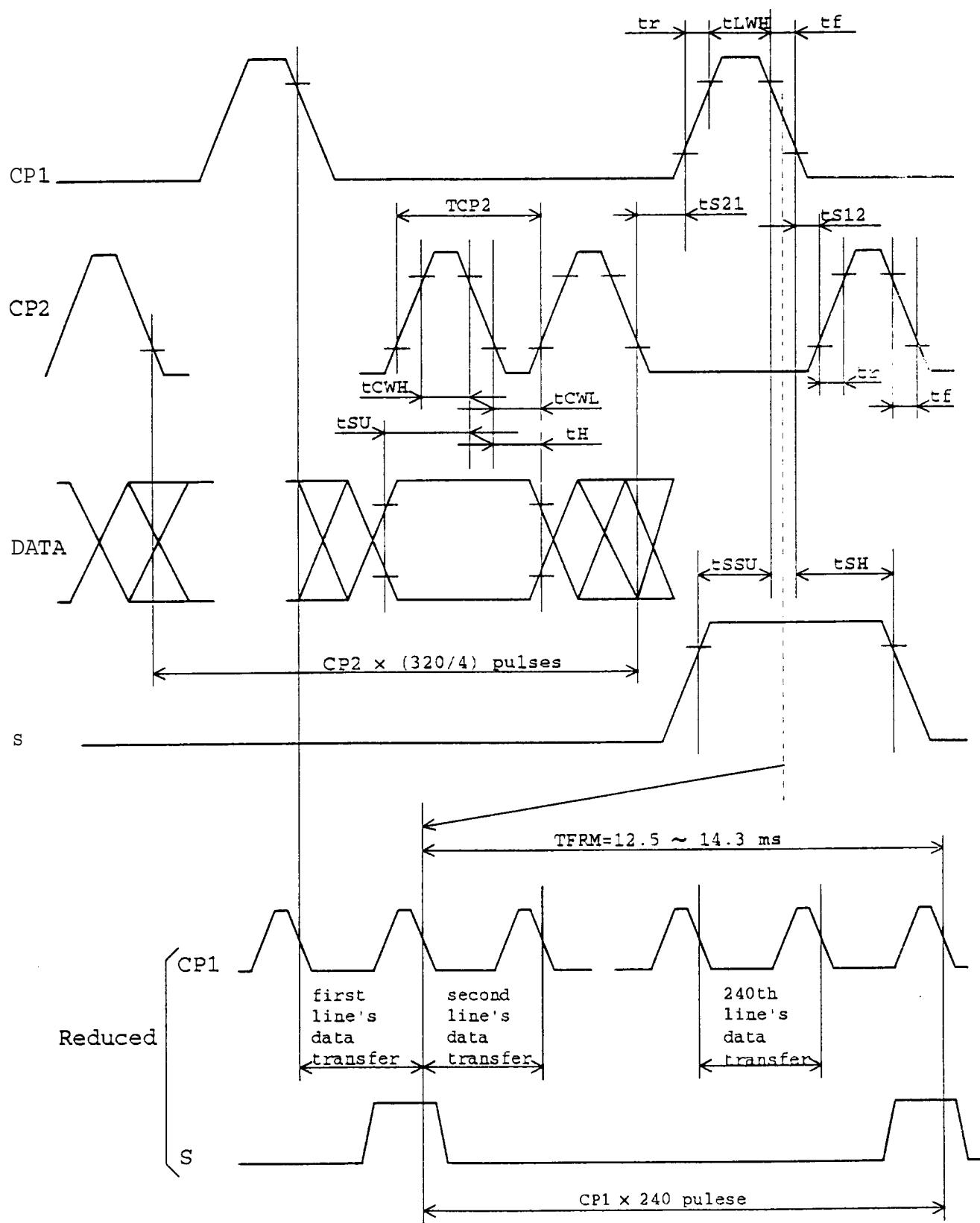


Fig.2 Data input timing chart



$V_{IH} = 0.8VDD$
 $V_{IL} = 0.2VDD$

Fig. 3 Interface timing chart

Table 7 Interface timing ratings

Item	Symbol	Rating			Unit
		MIN.	TYP.	MAX.	
Frame cycle Note 1)	tFRM	12.5		14.3	ms
CP2 clock cycle	tcp2	152			ns
"H" level clock width	tCWH	100			ns
"L" level clock width	tCWL	100			ns
"H" level latch clock width	tLWH	100			μs
Data set up time	tSu	80			μs
Data hold time	tH	80			ns
CP2T clock allowance time from CP1↓	tS12	0			ns
CP1↑ clock allowance time from CP2↓	tS21	0			ns
Input signal rise/fall time (Note 1)	tr, tf			trf	ns
S Signal Data set up time	tssu	100			ns
S Signal Data hold time	tSH	100			ns

(Note 1)

 $trf = 50 \text{ in case } tCT = (TCP2 - tCWH - tCWL) / 2 \geq 50$ $trf = tCT \text{ in case } tCT = (TCP2 - tCWH - tCWL) / 2 < 50$

6. Module driving method

6.1 Circuit configuration

Fig.4 shows the block diagram of the module's circuitry.

6.2 Display face configuration

The display consists of **320x240** dots as shown in Fig.1.

The interface is to be driven at **1/240** duty ratio.

6.3 Input Data and Control Signal

The LCD driver is 80 bits LSI, consisting of shift registers, latch circuits and LCD driver circuits. Input data for each row 320 will be sequentially transferred in the form of 4 bit parallel data through shift registers from **top left** of the display together with clock signal (CP2) .

When input of one row (320 dots) is completed, the data will be latched in the form of parallel data corresponding to the **signal electrodes** by the falling edge of latch signal (CP1) . Then, the corresponding drive signals will be transmitted to the 320 lines of **column electrodes** of the LCD panel by the LCD **drive** circuits.

At this time, scan start-up signal (S) has been transferred from the scan signal driver to the **1st row** of scan electrodes, and the contents of the data signals are displayed on the **1st row** of the display face according to the combinations of voltages applied to the scan and **signal electrodes** of the LCD. While the data of **1st row** are being displayed, the data of **2nd row** are entered. When data for 320 dots have been transferred, they will be latched by the falling edge of CP1, switching the display to the **2nd row**.

Such **data** input will be repeated up to the 240th row of each display segment, from upper row to lower rows, to complete one frame of display by time sharing method. then data input proceeds to the next display face.

Scan start-up Signal S generates scan signal to drive horizontal electrodes.

The module shall be driven at the speed of **70~80 Hz/frame** to avoid flickering.

Data" input for column electrodes of display segment and chip select of **driver** LSI are made as follow.

The driver LSI at the left end of the display face is first selected, and the adjacent driver LSI of the right side is selected when 80 dots data (20 CP2) is fed. This

process is sequentially continued until data is fed to the driver LSI at the right end of the display face.

This is simultaneously followed at the column driver LSI's of both the upper and the lower display segments. Thus data input through 4-bit bus line sequentially from the left end of the display face.

Since this graphic display module contains no refresh RAM, it requires data and timing pulse inputs even for static display.

The timing chart of input signals are shown in Fig.3

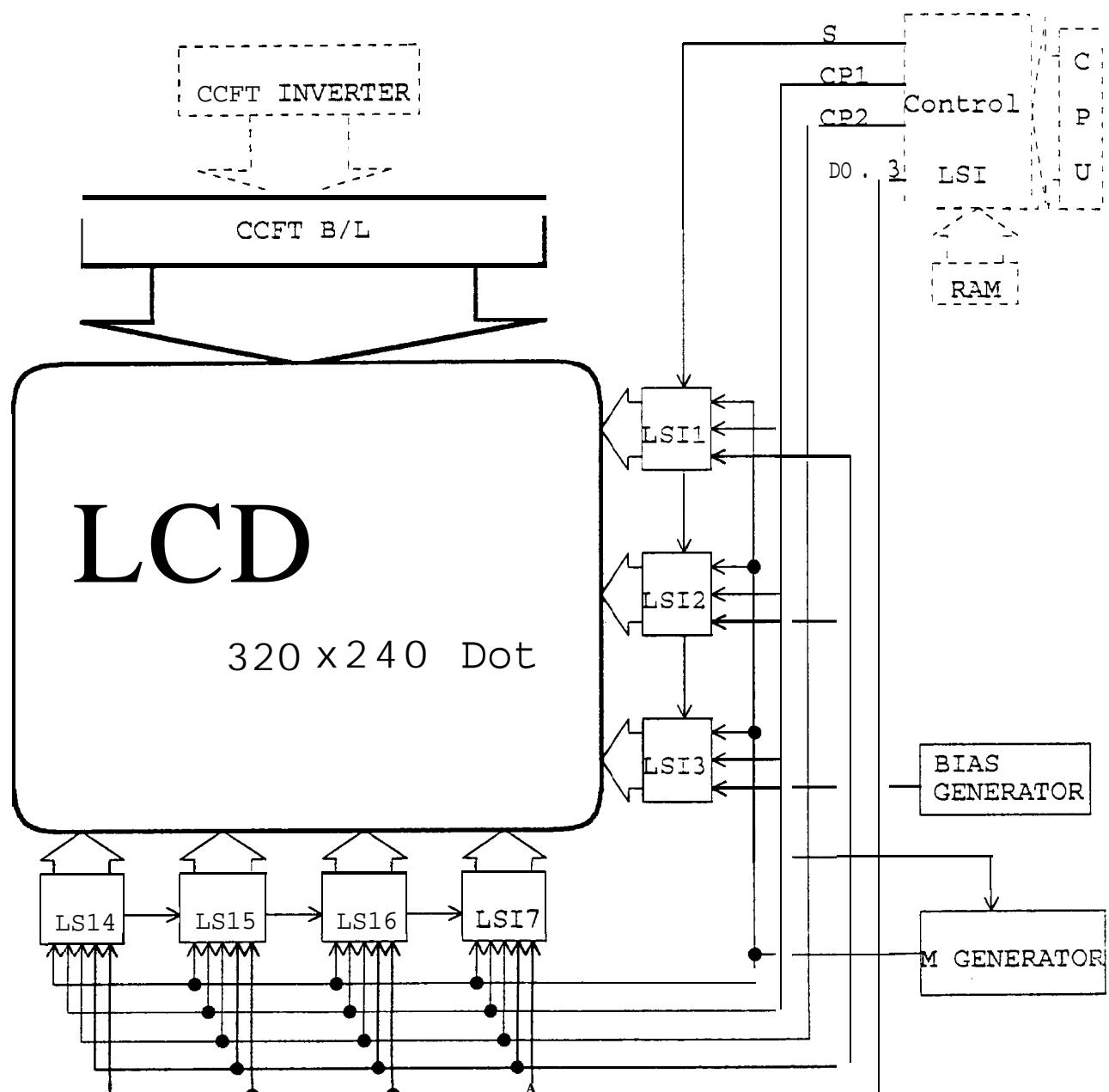


Fig.4 Circuit block diagram

" 7. Optical characteristics

Table 8

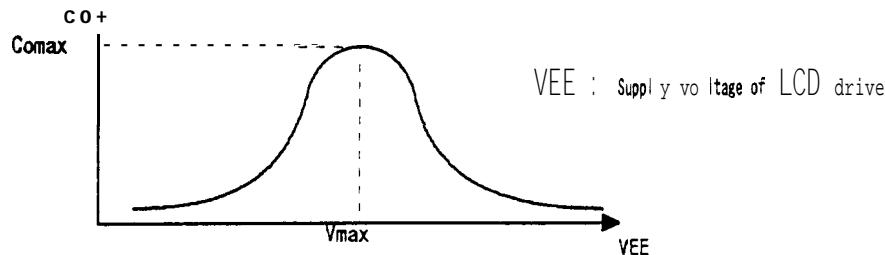
Ta=25 °C, 1/240 DUTY, VDD=5 V, VDD-VO=Vmax

Parameter	Symbol	Condition			MIN.	Typ.	MAX.	[Unit]	Remark
Viewing angle range	θ_x Transmissive mode	co>2.0	$\theta_y=0^\circ$	$\theta_x \geq 0^\circ$	-30	-	-	dgr.	Note 2
				$0^\circ < \theta_y < 0^\circ$	-	-	20	dgr.	
	θ_y Reflective mode	Co>2.0	$\theta_x=0^\circ$	$\theta_y \geq 0^\circ$	30	-	-	dgr.	Note 3
				$\theta_y < 0^\circ$	-	-	-20	dgr.	
			$\theta_x=0^\circ$	$\theta_y \geq 0^\circ$	30	-	-	dgr.	
				$\theta_y < 0^\circ$	-	-	-45	dgr.	
Contrast ratio	Transmissive	co	$\theta_x=\theta_y=0^\circ$		7	10	-		Note 1
	Reflective	co	$\theta_x=\theta_y=0^\circ$		6	8	-		
Response time	Rise	τ_r	$\theta_x=\theta_y=0^\circ$			250	375	ms	Note 4
	Decay	τ_d	$\theta_x=\theta_y=0^\circ$			440	660	ms	
Brightness		B			40	60	-	cd/m²	Note 3

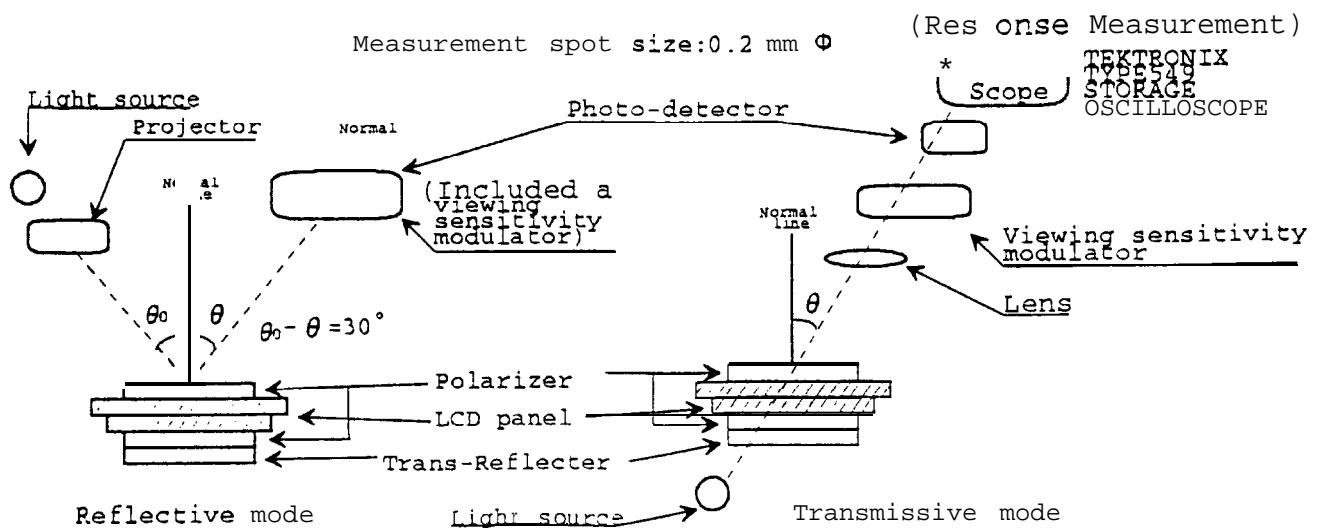
Note 1) Contrast ratio is defined as follows:

Vmax is defined as follows:

$$\text{Contrast} = \frac{\text{Luminance (brightness)}_{\text{all pixels "White" at Vmax}}}{\text{Luminance (brightness)}_{\text{all pixels "dark" at Vmax}}}$$

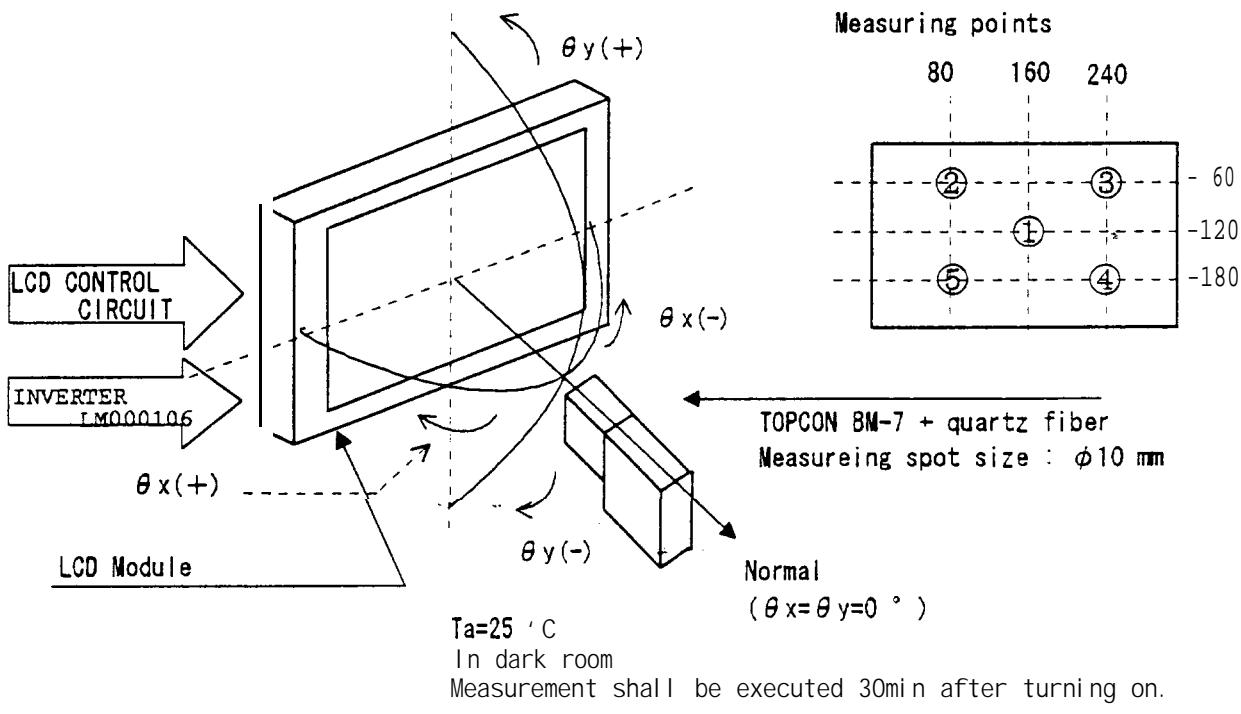


Optical Characteristics Test Method



Note 2) The viewing angle range is defined as shown Note 3.

Note 3) Measurement method of Viewing angle, Brightness

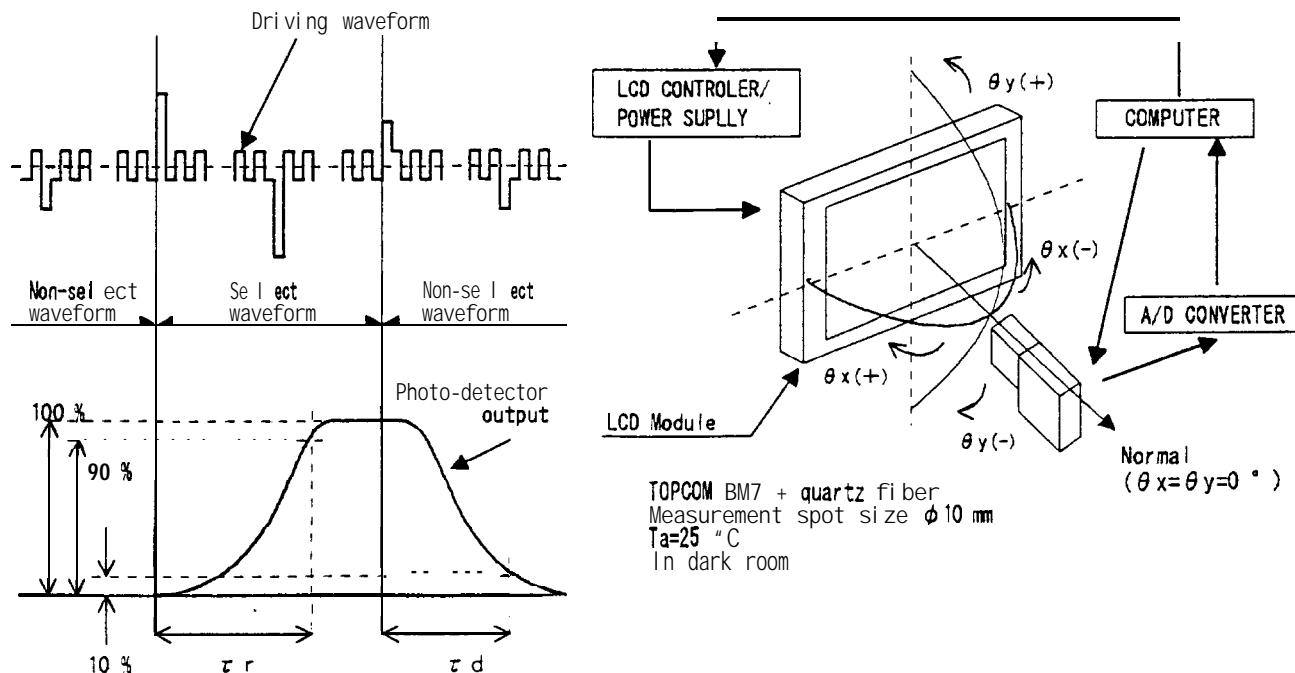


Measurement circuit : LM000106 (SHARP) (at $IL=5\text{mA rms}$)

Measurement equipment : BM-7 (TOPCOM)

Measurement circuit voltage : DC=12 V at primary side
LCD : ALL dots WHITE $V_{DD}=5\text{ V}$, $V_{DD}-V_0=V_{max}$

Note 4) Definition/Measurement method of Response time



8.Characteristics of Backlight

The ratings are given on condition that the following conditions are satisfied.

I)Rating (1pcs)

Table 9

Parameter	Symbol	MIN.	TYP .	MAX.	Unit	Remark
Brightness (B)	B	-	25 000	-	cd/m ²	Note 1 Note 2
Lamp voltage (AC/rms)	VL	250	275	300	v	Note 1 Note 2
Lamp current (AC/rms)	IL	4	5	6	mA	Note 1 Note 2
Kick-off voltage (AC/rms)	Vs	780	-		v	Note 1 Note 2
Power consumption	w	-	1.38	-	W	Note 1 Note 2, Note 3

Note 1) This value means CCFT lamp only.

Note 2) Measurement conditions

Measurement circuit : LM000106 (SHARP)
(at IL=5 mA rms)

Measurement equipment: BM-7 (TOPCOM)

Measurement circuit voltage
: DC=12 V at primary side

Measurement shall be executed 30 minutes
after turning on.

Note 3) Power consumption is calculated reference value.

(IL×VL, excluded inverter loss.)

Note 4) Within no conductor closed. (CCFT only)

Note 4) It is recommended that IL be not more than 5 mA so
that heat radiation of CCFT backlight may least
affect the display quality.

2) Operating life

The operating life time is 10 000 h or more at 5 mA.

(Operating life with LM000106 or equivalent.)

The inverter should meet the following conditions to keep
the specified life time of used lamp;

- Sine, symmetric waveform without spike in positive and negative.

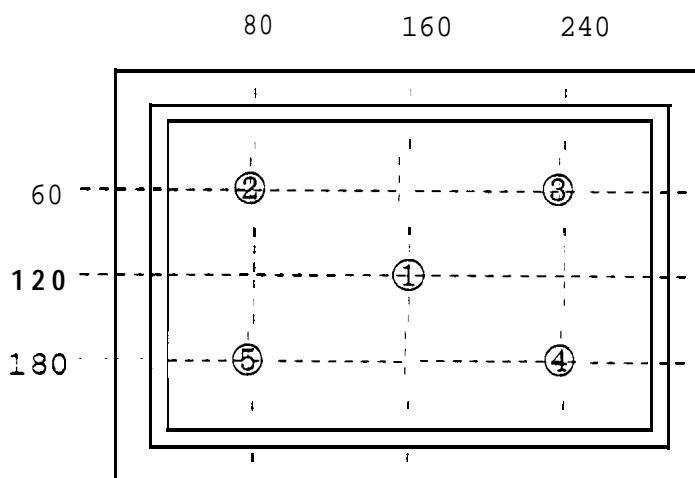
The operating life time is defined as having ended when **any**
of the following conditions occur; 25±5 °C

When the voltage required for initial discharge has
reached 110 % of the initial value.

- When the illuminance or quantity of light has decreased to 50 % of the initial value.

Note) Rating are defined as the average brightness inside the viewing area specified in Fig.5.

Fig.5 Measuring points (①~⑤)



9.Precautions

1) The module should be driven according to the specified ratings to avoid malfunction of permanent damage. DC voltage drive leads to rapid deterioration of LC, so ensure that the drive is alternating waveform by continuous application of the signal M.

Especially the power ON/OFF sequence shown on Fig.6 shall be followed to avoid latch-up of drive LSIS and application of DC voltage to LCD panel.

2) Industrial (Mechanical) design of the product in which this LCD module will be incorporated must be made that the viewing angle characteristics of the LCD may be optimized. Please consider the optimum viewing conditions according to the purpose when installing the module. (For the optical characteristics refer to the Table 8.)

3) This module is installed using mounting holes at the four corners of module. When installing the module, pay attention and handle carefully not to allow any undue stress such as twist or bend.

A transparent acrylic resin board or other type of protective panel should be attached to the front of the module to protect the polarizer, LCD cells, etc.

4) Since the front polarizer is easily damaged. Please pay attention not to scratch on its face.

5) If the **surface** of the LCD cells needs to be cleaned, wipe it swiftly with cotton or other soft cloth. If still not completely clear, blow on its and wipe.

6) Water droplets, etc., must be wiped off immediately since they may cause **color** changes, staining, etc. , if remained for a long time.

7) Since LCD is made of glass plates, dropping the **module** or banging it against hard objects may cause **cracking** or fragmentation.

8) CMOS LSIS are equipped in this module, so **care** must be taken to avoid the **electro** static charge, by **earthing** human body, etc.

9) Avoid to expose the module to the direct sun-light, strong ultraviolet light, etc. for a long time.

10) If stored at temperatures below specified storage temperature, the LC may freeze and be deteriorated. If storage temperatures exceed the specified rating, the molecular orientation of the LC may change to that of a liquid, and they may not revert to their original state.

11) Disassembling the LCD module can cause permanent damage and should be strictly avoided.

12) Don't use any materials that emit gas from epoxy resin (amines'herdener) and silicone adhesive agent (**dealcohol** or **deoxym**) to prevent change polarizer color owing to gas.

10. Applicable inspection standard

The LCD module shall meet the following inspection standard :**S-U-012-01**.

11. This specification describes display quality in case of no gray scale. Since display quality can be affected by gray scale methods, display quality shall be carefully evaluated for the usability of the LCD module in case gray scale is displayed on the LCD module.

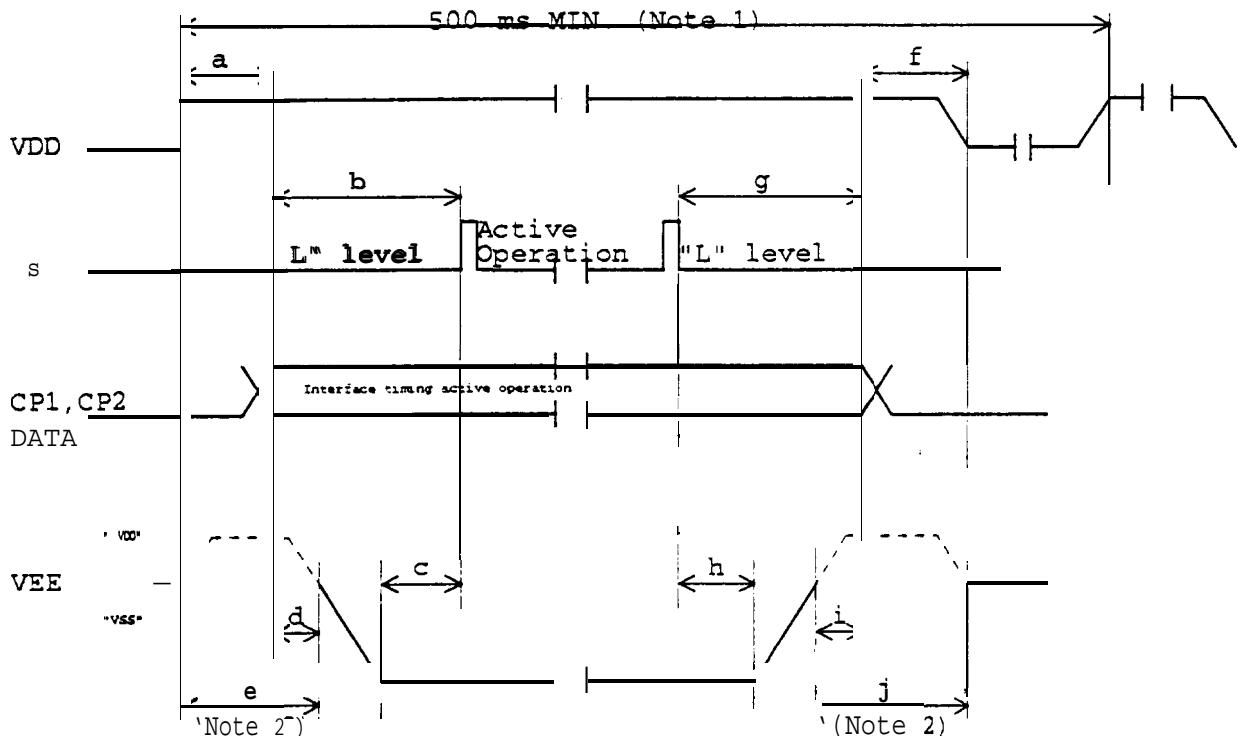


Fig 6 Sequence condition

Supply voltage sequence condition

SYMBOL		SYMBOL	
a	0 ms MIN, 20 ms MAX.	f	0 ms MIN, 20 ms MAX.
b	20 ms MIN.	g	20 ms MAX.
c	0 ms MIN.	h	0 ms MIN.
d	0 ms MIN, 100 ms MAX.	i	100 ms MIN.
e	(Note 2)	j	(Note 2)

Note 1) Power ON/OFF cycle time. All signals and power line shall be in accordance with above sequence in case of power ON/OFF.

Note 2) VEE to be set at "VDD level" or "open". VEE should be in accordance with the dotted line.

図面番号
DRAWING NO.
NO. 1
新規
NEW
変更
CHANGE
削除
DELETE
置換
REPLACE

170+0.5

160-0.5

7.5

150+5
-0.5

Note 3
PIN1
0.00
0.00
1.1

4.5
(0.6)

4-R1

1.1
17

1.21

1.16

1.15

1.14

1.13

1.12

1.11

1.10

1.09

1.08

1.07

1.06

1.05

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1.03

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